UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,278	07/14/2003	Lei Wu	MP0227	6329

45641 7590 04/19/2007

THE LAW OFFICES OF ANDREW D. FORTNEY, PH.D., P.C.
401 W. FALLBROOK AVENUE
SUITE 204
FRESNO, CA 93711-5835

EXAMINER	
TRAN, KHANH C	
ART UNIT	**PAPER NUMBER**
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/619,278	WU ET AL.	
	Examiner	Art Unit	
	Khanh Tran	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36,38-42,44-63,65-76 and 78-83* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6, 9-20,22-26,28-36, 38-42 are 44-59* is/are allowed.

6)☒ Claim(s) *1,7-8,60-63,65-76 and 78* is/are rejected.

7)☒ Claim(s) *2-5,21,27 and 79-83* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The Amendment filed on 01/25/2007 has been entered. Claims 1-36, 38-42, 44-63, 65-76 and 78-83 are pending in this Office action.

Response to Arguments

2. Applicant's arguments, see Applicants' Remarks on pages 15-16, filed on 01/25/2007, with respect to the rejection(s) of claim(s) 1-9, 15-42, 44-63 and 65-76 under 35 U.S.C 102(b) and 35 U.S.C 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Wolaver U.S. Patent 4,590,602.

Claim Objections

3. Claim 21 is objected to because of the following informalities: in line 2, "clock data recovery circuit" should be changed to -- clock recovery adjustment circuit --; in line 3, "clock data recovery circuit" should be changed to -- clock recovery adjustment circuit --; in line 5, "clock data recovery circuit" should be changed to -- clock recovery adjustment circuit --. Appropriate correction is required.

4. Claim 27 is objected to because of the following informalities: in line 6, "said data stream" should be changed to -- a data stream --. Appropriate correction is required.

5. Claim 79 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 2. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 60-61, 65 and 68-72 are rejected under 35 U.S.C. 102(b) as being anticipated by Wolaver U.S. Patent 4,590,602.

Regarding claim 1, in column 4 lines 10-3060, FIG. 1, which illustrates a preferred embodiment of the present invention, shows a block diagram of a wide range clock recovery circuit 100 having data input means, clock recovery phase lock loop (PLL) means, and wide range frequency synthesizer means.

The PLL means includes phase detector means 20, lock detector means 30, loop filter means 40, and wide range voltage controlled oscillator (VCO) means 50. The PLL means corresponds to the claimed clock phase adjustment circuit, for receiving the clock phase information of the NRZ data and providing a clock phase adjustment circuit; see FIG. 1.

The wide range frequency synthesizer means includes reference signal oscillator means 60, frequency divider means 70, frequency detector means 80, loop filter means 40, wide range VCO means 50, and range selector means 90. The wide range frequency synthesizer means corresponds to the claimed clock frequency adjustment for receiving clock frequency information and providing a clock frequency adjustment signal; see FIG. 1.

As recited above, the combination of phase detector means 20 and frequency detector means 80, which correspond to the claimed logic. Phase detector means 20 and frequency detector means 80 sample data stream at predetermined times, receive a plurality of predetermined phases of the clock signal (see FIG. 5) and provide clock frequency information and clock phase information from sampled data and predetermined phases of the clock signal.

FIG. 1 further discloses an adder, receiving the clock phase adjustment signal and the clock frequency adjustment signal to provide a clock recovery adjustment signal; see FIG. 1.

Regarding claim 60, claim is rejected on the same ground as for claim 1 because of similar scope. Furthermore, as recited in claim 1 rejection, the wide range frequency synthesizer means includes reference signal oscillator means 60. In column 7 line 65 via column 8 line 10, if the user input of m has brought f_o to within +/-1% of the input data rate and the seize bandwidth of the PLL means has been selected to also be +/-1%, the PLL means will seize, and lock detector means 30 will output an inhibit signal to frequency detector means 80 along line 32 which disables the operation of the frequency synthesizer means portion of the circuit. Furthermore, If, for example, the input data rate or the frequency synthesizer means' estimate of that data rate is less than any frequency in that window, then the auto-ranging means divides down the narrow range VCO frequency by some predetermined factor so as to create a lower frequency window and then checks to see if the estimated or input data rate is within this range. When the appropriate frequency range is found, the VCO means is tuned to output the estimated frequency. In view of the foregoing, because the clock recovery circuit would stop when the lock detector means 30 outputs an inhibit signal, the clock frequency information and clock phase information are generated by comparing data sampled at least two or more successive phase of the reference signal oscillator means 60.

Regarding claim 61, as recited in claim 1 rejection, phase detector means 20 and frequency detector means 80 sample data stream at predetermined intervals. As known

in the art that phase detector means 20 and frequency detector means 80 can be implemented as flip-flops to latch the data stream at predetermined intervals.

Regarding claim 65, phase detector means 20 and frequency detector means 80 samples data continuously until lock detector means 30 will output an inhibit signal to frequency detector means 80 along line 32 which disables the operation of the frequency synthesizer means portion of the circuit.

Regarding claim 68, as recited in claim 60 rejection, the wide range frequency synthesizer means includes reference signal oscillator means 60. In column 7 line 65 via column 8 line 10, if the user input of m has brought f_o to within +/-1% of the input data rate and the seize bandwidth of the PLL means has been selected to also be +/-1%, the PLL means will seize, and lock detector means 30 will output an inhibit signal to frequency detector means 80 along line 32 which disables the operation of the frequency synthesizer means portion of the circuit. Furthermore, If, for example, the input data rate or the frequency synthesizer means' estimate of that data rate is less than any frequency in that window, then the auto-ranging means divides down the narrow range VCO frequency by some predetermined factor so as to create a lower frequency window and then checks to see if the estimated or input data rate is within this range. When the appropriate frequency range is found, the VCO means is tuned to output the estimated frequency. Hence, the process is repeated until the lock detector outputs an inhibit signal.

Regarding claim 69, in addition to claim 68 rejection, depending the input data rate, different reference clock phase and frequency is selected to perform autoranging.

Regarding claim 70, referring to FIG. 1, the frequency synthesizer means adjusts the clock frequency information based on the frequency tuning range by applying program frequency divider coefficient m.

Regarding claim 71, claim is rejected on the same ground as for claim 70 because of similar scope.

Regarding claim 72, referring to FIG. 1, both the clock phase and clock frequency are altered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 7-8, 62-63 and 66-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolaver U.S. Patent 4,590,602.

Regarding claim 7, Wolaver does not expressly disclose the clock frequency information comprising an undershoot determination and an overshoot determination as set forth in the application claim.

However, in column 3 lines 40-55, Wolaver discloses that to permit single loop realization of such a wide range clock recovery circuit at high frequencies, a wide range VCO means is provided having an auto-ranging means. If, for example, the input data rate or the frequency synthesizer means' estimate of that data rate is less than any frequency in that window, then the auto-ranging means divides down the narrow range VCO frequency by some predetermined factor so as to create a lower frequency window and then checks to see if the estimated or input data rate is within this range. When the appropriate frequency range is found, the VCO means is tuned to output the estimated frequency. Because the input frequency is always tuned within a range of tunable frequencies, one of ordinary skill in the art at the time the invention was made would have recognized that the clock frequency information comprises an undershoot determination and an overshoot determination.

Regarding claim 8, Wolaver does not expressly disclose the clock phase information comprising an early clock phase determination and a late clock phase determination as set forth in the application claim.

However, because the PLL means employs a phase detector means 20 to compare the input phase and the feedback phase to produce a correct phase signal, one of ordinary skill in the art at the time the invention was made would have

recognized that the input clock phase information comprises an early clock phase determination and a late clock phase determination.

Regarding claim 62, Wolaver does not expressly disclose the predetermined intervals are less than two-data bit lengths as claimed in the application claim.

Referring to FIG. 1, the phase of a particular bit passes through phase detector means 20 and correction signal V_0 is produced and fed back to phase detector means 20 for comparing the phase with the next input bit. Because the phase comparison is performed between the current bit and the previous bit, one of ordinary skill in the art at the time the invention was made would have recognized that the sampling of phase detector means 20 is performed at every 1 data bit length.

Regarding claim 63, claim limitation has been addressed in claim 62 rejection.

Regarding claim 66, Wolaver does not expressly disclose the sampling is performed periodically as claimed in the application claim.

Because, as recited in claim 60 rejection, the operation of the PLL means and the frequency synthesizer means portion of the circuit will seize when lock detector means 30 outputs an inhibit signal, one of ordinary skill in the art at the time the invention was made would have recognized that the sampling process of the PLL means and the frequency synthesizer means is performed periodically.

Regarding claim 67, claim is rejected on the same ground as for claim 66 because of similar scope.

8. Claims 73-76 and 78 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolaver U.S. Patent 4,590,602 in view of admitted prior art in FIG. 2.

Regarding claim 73, claim is rejected on the same ground as for claim 60 because of similar scope.

Wolaver, however, does not discuss adjusting a frequency of a second clock signal in response to at least said clock frequency information as claimed in the application claim.

FIG. 2 admitted prior art illustrates a transceiver in which the frequency of the recovered clock is employed to adjust the frequency of the function generator 112 on the transmitter side.

Wolaver teaches a clock signal recovery circuit for a digital data communications receiver. As known in the art, a communications system includes a transmitter and receiver. Because Wolaver teachings provides a clock recovery circuit from variable rate data streams over a wide range of frequencies, it would have been obvious for one of ordinary skill in the art at the time the invention was made would have been motivated to implement Wolaver teachings in the transceiver as discussed in FIG. 2 admitted prior art.

Regarding claim 74, the clock recovery circuit of FIG. 1 of Wolaver invention further produces the clock signal V_0.

Regarding claim 75, the phase detector as shown in FIG. 2 admitted prior art provides data signal RXD; see paragraph [0006] of the original disclosure.

Regarding claim 76, claim is rejected on the same ground as for claim 68 because of similar scope.

Regarding claim 78, FIG. 2 admitted prior art discloses the FOFFSET_LPF adjusting the phase of the function signal.

Allowable Subject Matter

9. Claims 2-5 and 80-83 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claims 6, 9-36, 38-42 are 44-59 are allowed.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KCT

Khanh Cong Tran

04/13/2007
Khanh Tran
Primary Examiner, AU 2611